said central processor controlling said graphics processor and said sound processor based on said electrical information from said man-machine interface and a program code in said software;

said graphics processor having means to generate image information, and said sound processor having means to generate sound information.

4. (Amended) An information processing apparatus according to claim 3, wherein said information processor has a central processor, a graphics processor and a sound processor, said central processor, graphics processor and sound processor being connected to a common bus to which said semiconductor memory is connected;

said central processor, said graphics processor and said sound processor sharing a memory space in which said semiconductor memory is allocated, and sharing said semiconductor memory as bus masters;

said central processor controlling said graphic processor and said sound processor based on said electrical information from said man-machine interface and a program code in said software;

said graphics processor having means to generate image information; and said sound processor having means to generate sound information.

REMARKS

The Office Action dated July 26, 2002 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Claims 2 and 4 are amended. No new matter is added. In view of the above amendments and the following remarks, favorable consideration of claims 1-8 is respectfully requested.

